the sum of the utmost outer periphery pair is smaller than that of another pair of the periphery region.

5. The device according to claim 1, wherein

the first region in each of the center and the periphery regions has a constant impurity concentration,

the second region in each of the center and the periphery regions has a constant impurity concentration,

the second region in each of the center and the periphery regions has a constant width in a repeat direction of the first and the second regions, and

the difference between the second impurity amount and the first impurity amount is controlled by a width of the first region in the repeat direction in each of the center and the periphery regions.

6. The device according to claim 5, wherein

the first region of the utmost outer periphery pair in the periphery region has a width, which is larger than a minimum width of the first region of another pair of the periphery region, and

the first region of the utmost inner periphery pair in the periphery region has a width, which is smaller than a width of the first region of a pair of the center region.

7. The device according to claim 6, wherein

the first region of the utmost outer periphery pair in the periphery region has a width, which is larger than a width of the first region of another pair of the periphery region, and

the first region of the utmost inner periphery pair in the periphery region has a width, which is smaller than a width of the first region of a pair of the center region.

8. A method for manufacturing a semiconductor device, which includes a semiconductor layer having a first region and a second region, wherein the first region has a first conductive type and the second region has a second conductive type, wherein the first and the second regions extend in a thickness direction of the device, wherein the first and the second regions are repeated alternately in a plane perpendicular to the thickness direction, the method comprising the steps of:

forming a mask on a semiconductor wafer having the first conductive type, wherein the mask includes a center region mask, an inner periphery region mask and an outer periphery region mask, wherein the center region mask has a plurality of openings, each distance of which is constant, wherein the inner periphery region mask has a plurality of openings, each distance of which is smaller than the distance of the openings of the center region mask, wherein the outer periphery region mask has a plurality of openings, each distance of which is larger than the distance of the openings of the inner periphery region mask;

forming a plurality of trenches on the semiconductor wafer through the openings of the mask by an anisotropic etching method; and

forming a semiconductor region having the second conductive type in each trench.

9. The method according to claim 7, wherein

the center region mask is disposed at a center portion of the semiconductor wafer,

the inner periphery region mask surrounds the center region mask, and

the outer periphery region mask surrounds the inner periphery region mask.

10. The method according to claim 7, wherein

the semiconductor region having the second conductive type in each trench provides the second region, and

the semiconductor wafer is divided into a plurality of portions in the step of forming the trenches so that the plurality of portions provide the first regions, respectively.

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